IN THE SPECIFICATION

Please replace the paragraph at page 9, lines 11-13, with the following rewritten paragraph:

Figure 17(A) is a cross-sectional end view taken along the same direction as in Figure 12(A) at the step subsequent to the step in Figure ~~17~~ 16.

Please replace the paragraph at page 9, lines 21-23, with the following rewritten paragraph:

Figure 19(A) is a cross-sectional end view taken along the same direction as in Figure 12(A) at the step subsequent to the step in Figure ~~19~~ 18.

Please replace the paragraph at page 14, line 22 to page 15, line 5, with the following rewritten paragraph:

As shown in Figures 4(A) and 4(B), after removing the doping mask by a hydrofluoric acid, an oxide film and a nitride film are then continuously deposited to form an insulation film 4, patterning is performed by the electron beam lithography, and a hard mask composed of an insulation film 4 is formed by the RIE. A silicon wall vertical to the substrate 1 is then formed on the right side of the channel 5 by the crystal anisotropic (orientation-dependent) wet-etching or RIE. At this time, each of the source region 7-1 and drain region 7-2 is simultaneously shaped on one side thereof. With this state maintained, as shown in Figures 5(A) and 5(B), a gate insulation film 6-2 that will finally be a relatively thick gate insulation film is formed by the thermal oxidation or Chemical Vapor Deposition (CVD). In this process, though a silicon dioxide film is actually formed on each side of the source and drain 7-1 and 7-2, it is not shown in the drawings.

Please replace the paragraph at page 15, line 20 to page 16, line 8, with the following rewritten paragraph:

As shown in Figures 6(A) and 6(B), a resist pattern 10 is formed by the electron beam lithography, for example. What is important here is that the resist pattern 10 covers the thick gate oxide film 6-2 already formed and extends leftward by the channel thickness (a thickness toward the pair of gate electrodes). For this, though alignment with nanoscale precision is required in this process, this problem can satisfactorily be solved with the existing technique. After the formation of the resist pattern 10, a hard mask composed of an insulation film 4 is formed, the silicon layer is etched by the crystal anisotropic (orientation-dependent) wet-etching or RIE to form a vertical silicon wall on the left side of the channel 5, and a thin gate oxide film is formed by a short-time thermal oxidation, as shown in Figures 7(A) and 7(B). In this step, as described earlier with reference to Figure 5(A), the permittivity-changing step of depositing an aforementioned appropriate material as shown by virtual arrows f may be taken relative to either one of the gate insulation films, i.e. the thick gate insulation film 6-2, for example. Where the permittivity-changing step is taken similarly in this step relative to the thinner gate insulation film 6-1, an appropriate dielectric material is deposited in the opposite direction obliquely across the channel.

Please replace the paragraph at page 17, lines 14-22, with the following rewritten paragraph:

In either the case of providing the gate electrodes 3-1 and 3-2 with a difference in work function or the case of providing them with no difference, in order to make planar regions of the gate electrodes determinate finally after the step shown in Figure 8, as shown in Figures 9(A) and 9(B), silicade glass 11 is deposited by the low-pressure ~~CVD~~ chemical vapor deposition (LPCVD), a gate pattern is formed by the electron beam lithography, and a

hard mask composed of silicade mask 11 is formed by RIE. Utilizing the hard mask, the gate material 3a is vertically etched to the buried oxide film 2 by RIE. Then, the gate oxide layers at the sidewalls of source-drain extension regions 6-1 and 6-2 are etched out with a diluted hydrofluoric acid.

Please replace the paragraph at page 17, line 23 to page 18, line 5, with the following rewritten paragraph:

After completion of the fabrication of the structure described above, a Phosphorus-doped Silicade Glass (PSG) for an n-type channel, a Boron-doped Silicade Glass (BSG) for a p-type channel and a Non-doped Silicade Glass (NSG) for both types of channels are continuously deposited to form an insulation film 8 as shown in Figures 10(A) and 10(B). Then a Rapid Thermal Annealing (RTA) is performed for diffusing impurities from the PSG or BSG insulation films into the source-drain extension regions at the opposite ends of the channel are doped. The insulation film is polished, with the insulation film 4 as a stopper, by the Chemical Mechanical Polishing (CMP), and the electrode material 3a is separated into a left gate electrode 3-1 and a right gate electrode 3-2 to obtain the dual-gate field effect transistor according to the specific manner of the present invention shown in Figure 1.

Please replace the paragraph at page 18, line 26 to page 19, line 9, with the following rewritten paragraph:

Figures 11(A) to 11(C) show a dual-gate field effect transistor according to another embodiment of the present invention. The different point from the field effect transistor of the present invention shown in Figure 1 is that, as best shown in Figure 11(B) that is a cross-sectional end view taken along line Y-Y in Figure 11(A), the cross section of a channel in the direction connecting the gate electrodes 3-1 and 3-2, i.e. the direction orthogonal to the

carrier-running direction (the cross section along line Y-Y) is triangular. This structure can be obtained through the use of an SOI substrate having (100) plane orientation and application of the crystal anisotropic (orientation-dependent) wet etching. An example of the production process will be described herein below. In Figures 12 to 20, the figures given (A) correspond to cross-sectional end views taken along line Y-Y in Figure 11, and the figures given (B) to cross-sectional end views taken along line X-X.

Please replace the paragraph at page 19, lines 10-16, with the following rewritten paragraph:

As shown in Figures 12(A) and 12(B), an SOI wafer having a silicon substrate provided with a buried oxide film 2 and a silicon crystal layer 5a is prepared. The surface thereof is thermally oxidized to form a silicon dioxide (SiO_2) film and, as shown in Figures 13(A) and 13(B), a doping mask is formed on the silicon dioxide film ~~is prepared~~ by using electron beam lithography and RIE. Then, regions where a source 7-1 and a drain 7-2 are to be formed are doped with appropriate impurities.

Please replace the paragraph at page 20, lines 9-24, with the following rewritten paragraph:

On the structure thus formed a resist pattern 10 is formed by electron beam lithography as shown in Figures 16(A) and 16(B) and, as shown in Figures 17(A) and 17(B), a hard mask composed of an insulation film 4 is formed by RIE, for example. Crystal anisotropic (orientation-dependent) wet etching is used to form an oblique silicon surface having a (111) plane orientation, which is subjected to a short-time thermal oxidation to form a thin gate oxide film ~~6-2~~ 6-1. As described earlier, when the permittivities of the pair of gate insulation films 6-1 and 6-2 are to be changed, in the step shown in Figure 17, a permittivity-

changing step by depositing an aforementioned appropriate material may be taken as shown by virtual arrows f relative to either one of the gate insulation films, i.e. the thick gate insulation film 6-2, for example, without taking the step shown in Figure 15 shown by virtual arrows f shown in Figure 15. Where the permittivity-changing step is taken similarly in this step relative to the thinner gate insulation film 6-1, an appropriate dielectric material is deposited in the opposite direction obliquely across the channel

Please replace the paragraph at page 21, line 28 to page 22, line 16, with the following rewritten paragraph:

After the step shown in Figure 19, as shown in Figures 20(A) and 20(B), PSG (BSG in the case of a p-type channel) and NSG are continuously deposited to form an insulation film 8. The insulation film is subjected to rapid thermal annealing and the impurities from the PSG or BSG are diffused into the source-drain extension regions to form doped channel extensions. The resultant is polished utilizing Chemical Mechanical Polishing (CMP), with the insulation film 4 used as a stopper to thereby complete a dual-gate field effect transistor having separated gate electrodes 3-1 and 3-2 according to the present invention as shown in Figure 11. As the subsequent treatments, the aforementioned treatments generally used in this kind of field are taken to complete a device as a product. In the case of using different metal materials to make the work functions of the pair of gate electrodes 3-1 and 3-2 different without the ion implantation, one of the gate electrodes is made from the first electrode material in the steps shown in Figures 18 and 19 and the other gate electrode is made from the second electrode material of different material and different work function from those of the first electrode material in the same manner. As the electrode materials to be combined, appropriate metal materials as described earlier may be selected.

Please replace the paragraph at page 22, line 27 to page 23, line 1, with the following rewritten paragraph:

The fabrication process of this structure may be the same as the process described with reference to Figures 12 to 20. The point to be made different is the time of the crystal anisotropic (orientation-dependent) wet etching in the step shown in Figures 17(A) and 17(B). The time is to be prolonged. The significant point is to accurately control the etching time.

Please replace the paragraph at page 23, line 22 to page 24, line 4, with the following rewritten paragraph:

Figure 23 shows the results of calculations in the embodiment described with reference to Figures 1 to 10, with the thickness t1 of the gate insulation film 6-1 fixed to 2 nm and the thickness t2 of the gate insulation film 6-2 varied from 2 nm to 20 nm. This shows the dependency of the subthreshold slope (right vertical axis: mV/dec.) and the threshold voltage (left vertical axis: V) on the gate voltage (lateral axis: Vgc) varying with a change in thickness of the gate insulation film t2, from which it is found that a transistor can be fabricated in accordance with the gist of the present invention while satisfactorily controlling the threshold voltage to a desired value. Figure 24 shows an example of the features showing the relationship between the subthreshold slope (~~right~~ left vertical axis: mV/dec.) and the threshold voltage (lateral axis: V).

Please replace the paragraph at page 25, lines 2-8, with the following rewritten paragraph:

For this reason, the aforementioned disadvantages in the conventional structure as shown in Figure 27 are eliminated or alleviated and, by adjusting the permittivities $\epsilon 1$ and $\epsilon 2$

of the gate insulation films during the device fabrication processes, a desirable threshold voltage within the range not increasing the subthreshold slope can be obtained even when the pair of gate electrodes 3-1 and 3-2 are electrically connected to each other and even when the respective potentials cannot be adjusted by gate-biasing independently.

Please replace the paragraph at page 29, lines 3-12, with the following rewritten paragraph:

Structurally, since not a planar channel shown in Figure 29, but a vertical channel is used, existing excellent fabrication techniques can effectively be utilized. For example, orientation-dependent wet etching technique can be used for the fabrication of vertical channels instead of the RIE. As a result, plasma-induced damage is not introduced into channels unlike the case where dry etching has to be used, and the channel surface can be provided with the (111) plane in a self-limited manner and flattened on the order of an atomic layer surface. Therefore, a high-performance field effect transistor exhibiting a small decrease in mobility by the channel surface roughness scattering can be obtained.

Please replace the paragraph at page 29, line 24 to page 30, line 7, with the following rewritten paragraph:

The present invention can contribute to reduction in power consumption in a dual-gate field effect transistor structure. Since the present invention provides means for freely controlling the threshold voltage to a great extent, with respect to the operation of a dual-gate field effect transistor, for example, the threshold voltage is lowered when necessary to guarantee high-speed operation and, at the standby time, the threshold voltage is raised to lower the off current, thereby making it possible to suppress the power consumption during the non-operation (standby state). Therefore, even in a semiconductor integrated circuit

comprising a plurality of the dual-gate transistors, not to mention a single unit of the device, there is no case where the performance thereof is lowered as compared with the conventional ones, and the power consumption can be suppressed to an optimum value while enhancing the performance of the device.